This listing of claims will replace all prior versions, and listings, of claims in the application:

**The Status of the Claims**

1. (Cancelled)

2. (Previously Amended) A method as defined in claim 3, wherein the spacers are formed by depositing and etching a SiN layer.

3. (Previously Amended) A method of fabricating a memory cell comprising:

forming spacers to isolate and protect a gate area including a floating gate and a control gate;

forming a gap filling layer over a substrate including the gate area and the spacers; and

depositing an insulating layer over the gate area and the gap filling layer, wherein the gap filling layer is formed by depositing undoped polysilicon or amorphous silicon over the gate area and the spacers, and by performing an anisotropic etching of the deposited undoped polysilicon or amorphous silicon.

4. (Previously Amended) A method as defined in claim 3, wherein the insulating layer is formed of TEOS (tetra ethyl ortho silicate) or BPSG (borophosphorsilicate glass).

5. (Cancelled)

6. (Previously Amended) A memory cell structure as defined in claim 7, wherein the spacers are formed of SiN.

7. (Previously Amended) A memory cell structure comprising:

a plurality of gate areas, the gate areas including a gate oxide, a floating gate, an insulating layer, and a control gate;

spacers on sidewalls of the gate areas;

a gap filling layer formed in gaps between the spacers of the gate areas; and

an insulating layer deposited over the gate areas and the gap filling layer, wherein the gap filling layer is formed of undoped polysilicon or amorphous silicon.

8. (Original) A memory cell structure as defined in claim 7, wherein the gap filling layer is formed by an anisotropic etching.

9. (Cancelled)

10. (Cancelled)